# Oscar Kellner

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https://github.com/Eightscer

## EDUCATION

Northeastern University, Boston, MA Expected May 2028
**Doctor of Philosophy in Computer Engineering** Current GPA: 4.000
Researching Computer Architecture in the Embedded Systems Laboratory
*Honors:* Dean's List
*Coursework:* **Operating Systems, Computer Architecture, Machine Learning,** High Performance Computing

Northeastern University, Boston, MA May 2023
**Bachelor of Science in Computer Engineering** GPA: 3.584
*Honors:* Dean's List, National Hispanic Recognition Program
*Coursework:* **Microprocessor-Based Design, Robotics, FPGA Hardware-Software Codesign,** Computer Architecture, Digital Design and Computer Organization, Embedded Design, Fundamentals of Engineering Algorithms, Fundamentals of Electronics, Fundamentals of Networks

## TECHNICAL SKILLS

***Programming Languages:*** C/C++, Zig, Python, Lua, Haskell
***Software:*** GCC, Embedded Systems (ARM), Linux Kernel Modules, Arduino
***Hardware:*** FPGAs, Vivado, High Level Synthesis, Verilog, Soldering
***Operating Systems:*** Linux, Mac OS X, Windows 10

## WORK EXPERIENCE

Bose, Framingham, MA Fall 2022
**FPGA and Software Development** (Co-op)

- Responsible for designing high-speed link-layer data transfer on embedded system through use of Aurora 64B/66B IP on Zynq Ultrascale+ and PetaLinux

## TECHNICAL PROJECTS

***System-level Design of Domain-Specific Accelerator for OpenVSX apps*** Fall 2023 - Current

- Automatically generate SystemC transaction-level modeling from application / architecture description obtained from Dm-TSAR-ILP

***Higher Order Machine*** Fall 2023 - Current

- High-level design and evaluation of a dataflow machine based off of an open-source, massively-parallel, pure functional runtime (HVM)

***Conv2D Hardware Accelerator*** Spring 2022

- Developed a direct convolution accelerator for 3x3 convolutions in C/C++ and synthesized using Vivado HLS, integrated with a modified machine learning framework (Darknet)
- Designed system integration using AXI-Stream and AXI4 DMA interfaces, realized on a Xilinx Zynq 7020 for a hardware/software co-design class project

***8-Bit Soft-core CPU*** Fall 2021

- Designed an 8-bit soft-core CPU in Verilog with a RISC-like ISA
- Realized as a Vivado RTL project on PYNQ and Arty-Z7 FPGA

***Embedded Real-time Game Demo*** Summer 2021

- Programmed a real-time video game in C++ on embedded system, wrote report for group project
- Utilized FPGA's built-in IO interfaces and clock through use of hardware documentation
- Incorporated graphics by writing to pixel buffer through VGA port and displayed on a monitor

## SKILLS AND INTERESTS

Trumpet, Music Tracking, ROM Hacking, Retrocomputing, Self-Hosting, Cooking